JEDEC
STANDARD

Guidelines for Reporting and Using Electronic Package Thermal Information

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Guidelines for Reporting and Using Electronic Package Thermal Information

(From JEDEC Board Ballot, JCB-05-68, formulated under the cognizance of the JC-15.1 Subcommittee on Thermal Characterization.)

1 Scope

This document provides guidelines for both reporting and using electronic package thermal information generated using JEDEC JESD51 standards. By addressing these two areas, this document can be used as the common basis for discussion between electronic package thermal information suppliers and users.

The first goal is for the electronic package thermal information to be reported consistently by different suppliers. Suppliers may choose to summarize the results or present a subset of the results, but the complete test information should be available on request. The complete information to be reported is documented in the various JESD51 standards, but key elements are consolidated in this guideline for easy reference by both suppliers and users.

The second goal is for end users to be able to properly understand, interpret and use the data reported. The purpose of the JESD51 standards is to compare the thermal performance of various packages under standardized test conditions. While standardized thermal test information cannot apply directly to the many specific applications, the standardized results can help compare the relative thermal performance of different packages. A more meaningful comparison is possible if the test conditions are understood along with the factors affecting package thermal performance. Brief discussions of key topics are included in this guideline.

2 Normative references

The following standards contain provisions that, through reference in this text, constitute provisions of this guideline. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on these standards are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below.

[1] JESD51, *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Devices)*. This is the overview document for this series of specifications.

[2] JESD51-1, *Integrated Circuit Thermal Measurement Method - Electrical Test Method*

[3] JESD51-2, *Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*

[4] JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

[5] JESD51-4, *Thermal Test Chip Guideline (Wire Bond Type Chip)*

[6] JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

[7] JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)*

[8] JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

[9] JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board*

2 Normative references (cont'd)

[10] JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

[11] JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

[12] JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

[13] JESDxx-yy, *JEDEC Two-Resistor Compact Model Standard* [in the ballot process at the time of publication]

[14] JESDxx-zz, *DELPHI Compact Model Guideline* [in the ballot process at the time of publication]

3 Terms, Definitions, symbols, and abbreviations

Standard JESD51 [1] is an overview document that introduces the electronic package thermal resistance concept. Most definitions and symbols are included in JESD51-1 [2], Annex A. JESD51-2 [3], Annex A includes definitions for the junction-to-top and top-to-air thermal characterization parameters. The junction-to-board thermal characterization parameter is introduced in JESD51-6 [7] and the junction-to-board thermal resistance test method is in JESD51-8 [9].

4 Reporting electronic package thermal results

The JEDEC JESD51 family of standards define the methodology necessary for making meaningful thermal measurements on packages containing single chip semiconductor devices. Different aspects of the methodology are defined in separate detailed standards. To measure one component thermal value the supplier follows one standard from each of the categories in Table 1.

The JEDEC Theta-JCx standard is under development. While Theta-JC measurements have been common for years (for example, Mil Std 883C Method 1012.1), it is very difficult to define a measurement method which provides accurate and repeatable results covering a wide range of package designs, sizes, and power dissipation. The nomenclature used in this document is consistent with the standard being developed. For the 2R model discussed in section 5.xx, the method by which Theta-JCtop was determined must be reported.

4 Reporting electronic package thermal results (cont'd)

Table 1 — JESD51 Thermal measurement standards by category

ENVIRONMENT[1]	CHIP	BOARD[4]	MEASUREMENT METHOD
• Natural Convection (Still Air), one cubic foot enclosure, θ_{JA}, Ψ_{JT} [3] [2] • Forced Convection (Moving Air), wind tunnel, θ_{JMA}, Ψ_{JT}, Ψ_{JB} [7] • Junction-to-Board, θ_{JB} [9] • Junction-to-Case, θ_{JCx} [3]	• Thermal Test Chip – Wire Bond Type [5] • Thermal Test Chip – Flip Chip Type (not yet available; refer to [5] for applicable information) • Active Die or Thermal Test Die [2]	• Low Effective Thermal Conductivity (1s board), Leaded Surface Mount Packages [4,6[5]] • High Effective Thermal Conductivity (2s2p board), Leaded Surface Mount Packages [8,6[4]] • Area Array Surface Mount Packages (1s and 2s2p boards) [10] • Through-Hole Perimeter Leaded Packages (1s and 2s2p boards) [11] • Through-Hole Area Array Leaded Packages (1s and 2s2p boards) [12]	• Static Mode or Dynamic Mode; Active Die or Thermal Test Die [2]

NOTE 1 In some cases the environment standards identify which test board cross-section (see note 3) is to be used when measuring a particular thermal value.

- θ_{JA} – the board used must be indicated [3]
- θ_{JMA} – 1s board, unless indicated otherwise [7]
- θ_{JB} – 2s2p board [9]; Ψ_{JB} is also normally measured on the 2s2p board [7]

A 1s board may not be practical for high lead count components. More discussion of the boards is included in Section 5.3.2.

NOTE 2 Ψ_{JB} was not included in the natural convection standard [3]; it had not yet been defined. It may be added in the future. Ψ_{JB} can be measured in the natural convection environment, but it is normally measured on a 2s2p board, and in the forced convection environment, including the zero forced convection condition [7].

NOTE 3 The JEDEC θ_{JCx} standard is under development. While θ_{JC} measurements have been common for years (for example, Mil Std 883C Method 1012.1), it is very difficult to define a measurement method which provides accurate and repeatable results covering a wide range of package designs, sizes, and power dissipation. The nomenclature used in this document (see section 5.2.2) is consistent with the standard being developed. For the 2R model discussed in section 5.2.4, the method by which θ_{JCtop} was determined must be reported

NOTE 4 Two test board cross-sections are defined in the JESD51 standards.

- The first cross-section is referred to as the low effective thermal conductivity or 1s board. The 1s refers to the one signal layer on the component side of the board, so the board is sometimes referred to as a single layer board. Limited signals are permitted on the opposite side actually making it a 2s or two layer board. The key point is that this board does not have power planes (0p). The signal layer traces are 0.070 mm (2 oz/ft^2) finished copper thickness.
- The second cross-section is referred to as the high effective thermal conductivity or 2s2p board. It has significantly more copper. The 2s refers to the signal layers on both outside surfaces of the board and the 2p refers to two power planes in the board (voltage and ground). The board is sometimes referred to as a four layer board. The signal layer traces are 0.070 mm (2 oz/ft^2) finished copper thickness and the power planes are 0.035 mm (1 oz/ft^2) finished copper thickness.
- For packages with ball pitch ≤ 0.5 mm the traces are reduced to 0.050 mm (1.5 oz/ft^2) finished copper thickness for both boards. [10]
- Test boards designed according to JEDEC JESD51 standards are referred to as JEDEC JESD51 boards or JESD51 boards. JEDEC does not make thermal test boards available.

NOTE 5 Reference [6] extends board standards [4] and [8] for packages with direct thermal attach mechanisms such as deep down-set exposed pad packages or thermally tabbed packages.

4 Reporting electronic package thermal results (cont'd)

Following a selected set of these standards allows the supplier to report the thermal information included in the Environment column. Each of the standards also has a table at the end that tells the component supplier what test condition information is to be reported for that aspect of the test. The following statement is from the JESD51 Overview, section 5:

> "Thermal data are not meaningful unless all pertinent test condition information is provided with the actual thermal data ... (The) documents for each of the measurement areas...state the thermal information necessary for a complete description of the data."

The tables in section 6 of this document identify some of the key elements from the standards that affect the thermal results.

Suppliers may choose to summarize the results or present a subset of the results, but the complete test information should be available on request. Suppliers may deviate from the JEDEC standards and still provide valuable data. Such deviations are to be identified.

When reporting information from tests run according to the JESD51 standards, suppliers are encouraged to indicate this in their reports and datasheets, together with any deviations. An example is given here.

> "This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org. Deviations from the JESD51 standards are noted on page xx."

5 Using standardized thermal results

5.1 General problems using standardized thermal results

Several factors affect the thermal performance of a device in a user's application. These include power dissipation in the component; airflow velocity, direction and turbulence level; power in adjacent components; two-sided vs. one-sided active component mounting; printed circuit board (PCB) orientation; and adjacent boards and their power dissipation.

Ways in which the JESD51 test condition may not match a specific application include

- Die size
- Printed circuit board size
- Amount of copper on the application boards vs. the JESD51 2s2p board
- Copper trace thickness – JESD51 0.070 mm (2 oz/ft^2) copper vs. application 0.018 mm (1/2 oz/ft^2) copper, for example
- Trace widths – JESD51 widths may be larger than trace widths in the application, for example
- Environment – JESD51 natural convection one cubic foot enclosure vs. a cell phone, for example
- Single heat source vs. multiple heat sources in the application

For specific applications, component and system level thermal engineers should be consulted. It may be necessary to test or model specific applications. This may require special thermal test vehicles involving application-specific boards and thermal test die.

Numerical modeling of the thermal performance of a component in a JESD51 standardized test can be used as a basis for modeling of the component in a specific application. To accomplish this, detailed package geometry and material information is required from the component supplier. Alternatively, the supplier may provide compact models that can be incorporated in numerical models (see section 5.2.4).

5 Using standardized thermal results (cont'd)

5.1 General problems using standardized thermal results (cont'd)

This testing and modeling of a component user's specific applications is the user's responsibility, but the work may be performed by component suppliers or consultants.

5.2 JESD51 standardized thermal values

The thermal resistances and thermal characterization parameters that are generated using JESD51 standards are described here together with their typical uses. All have the units of °C/W.

Reported results are generally average values. Standard deviation or range information may be available in some cases, or on request.

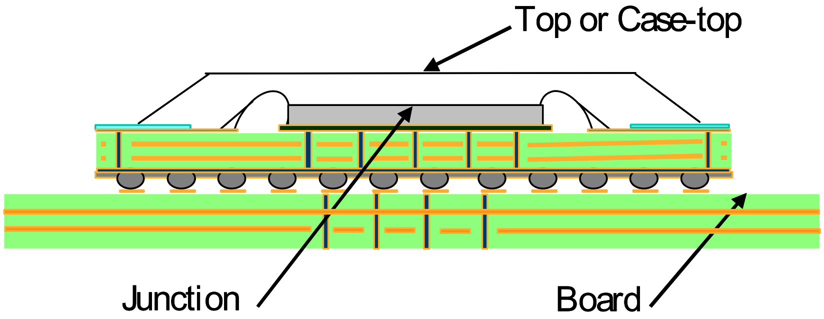

Figure 1 — Typical temperature location designations

Temperature measurement locations used to determine the thermal values are shown in Figure 1. The junction designation represents the location of the temperature sensitive device in the die used for the measurements [2]. User application dies may have an additional temperature rise from this representative junction to a hot-spot junction. The top, or case-top, and board designations are discussed in sections 5.2.2 and 5.2.3.

5.2.1 θ_{JA} and θ_{JMA} convection thermal resistances

The convection thermal resistances θ_{JA} (Theta-JA) and θ_{JMA} (Theta-JMA) are the chip junction-to-ambient air and junction-to-moving air thermal resistances measured in the convection environments described below. The values can be used to compare the thermal performance of different packages if all the test conditions listed in section 6 are similar.

θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure as described in [3] (the board type used must be indicated). This environment is sometimes referred to as "still air" although natural convection causes the air to move.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

P is the total power (heat) dissipated in the chip.

θ_{JMA} is the forced convection junction-to-moving air thermal resistance measured in a wind tunnel using a 1s board (unless indicated otherwise) as described in [7]. The equation is the same as for θ_{JA} but results are reported as a function of air velocity. A sample plot is given in Figure 4 on page 9.

5.2 JESD51 standardized thermal values (cont'd)

5.2.1 θ_{JA} and θ_{JMA} convection thermal resistances (cont'd)

The θ_{JA} and θ_{JMA} values are sometime used to estimate how a package will perform in a specific application. These estimates cannot be accurate because a standardized test condition cannot match the user's application condition. The reasons for this and how to deal with this situation have been described in section 5.1.

Similarly, the combination of system air temperature measurements together with θ_{JA} and θ_{JMA} values cannot be used to verify that a component junction temperature specification is met. To accomplish this, see section 5.2.3.

Some suppliers deviate from the JEDEC terminology by not using the θ_{JMA} symbol and instead reporting the θ_{JMA} information as "θ_{JA}" vs. velocity. This causes unnecessary confusion.

A θ_{JMA} value at zero forced velocity can be measured if the wind tunnel air moving device is turned off and the component is left in the wind tunnel. This value will be close to the θ_{JA} value measured in the one cubic foot enclosure if the 1s single layer board is used, and the board is mounted horizontally in a horizontal wind tunnel, and the wind tunnel has a cross-section close to 305 mm x 305 mm (one foot by one foot). Sometimes this θ_{JMA} value at zero forced velocity is reported as "θ_{JA}"; this should be noted as a deviation from the JESD51 standards.

5.2.2 θ_{JC} and θ_{JB} conduction thermal resistances

The conduction thermal resistances θ_{JCx} (Theta-JCx) and θ_{JB} (Theta-JB) are measured with nearly all of the component power dissipation flowing through either the top or the bottom of the package. The values may be useful for comparing packages but the test conditions don't generally match the user's application. An exception is an application where nearly all of the component heat is flowing through the top of the package to a heat sink. θ_{JCtop} is representative of this application.

The θ_{JCtop} and θ_{JB} resistances may be used in two resistor compact models as explained in JESDxx-yy [13] and described briefly in section 5.2.4 of this guideline.

θ_{JCx} is the junction-to-case thermal resistance. The "x" indicates the case surface where T_{Case} is measured and through which the heat is forced to flow during the θ_{JCx} measurement, "top" for the top surface or "bot" for the bottom surface. The surface used is typically that in the primary package heat transfer path and that is generally the top surface of the package, but not always. For example, for a thermally tabbed package the case is the bottom tab which is soldered to the circuit board during use.

$$\theta_{JCx} = \frac{T_J - T_{Case}}{P}$$

P is the part of the chip power (heat) that flows from the junction to the "x" case surface. Ideally, during θ_{JCx} measurement, close to 100% of the power flows from the junction to the "x" case surface.

The θ_{JCx} nomenclature is used to avoid the confusion associated with θ_{JC}. Historically, the θ_{JC} case surface is defined as the "outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk" [2]. This could be either the top or bottom surface, but it is not always clear which surface was used when a θ_{JC} value is reported.

5.2 JESD51 standardized thermal values (cont'd)

5.2.2 θ_{JC} and θ_{JB} conduction thermal resistances (cont'd)

θ_{JB} is the junction-to-board thermal resistance where T_{Board} is the temperature measured on or near the component lead, using a 2s2p board, as described in [9]. For a leaded package, the thermocouple is attached to the foot of a lead. For an area array surface mount package, the thermocouple is attached to a board trace within 1 mm of the package body.

$$\theta_{JB} = \frac{T_J - T_{Board}}{P}$$

P is the part of the chip power (heat) that flows from the junction to the board. Ideally, during θ_{JB} measurement using the test fixture in [9], close to 100% of the power flows from the junction to the board. The thermal conductivity of the board affects the results. The 2s2p boards with the higher thermal conductivity are used to provide consistent results and to approximate several common application environments.

5.2.3 Ψ_{JT} and Ψ_{JB} thermal characterization parameters

The thermal characterization parameters Ψ_{JT} (Psi-JT) and Ψ_{JB} (Psi-JB) are measured by suppliers at the same time and in the same environments as θ_{JA} or θ_{JMA}. Users can apply the Ψ (Psi) equations to estimate the component junction temperature in their application by measuring a component temperature in the application environment and using the appropriate Ψ thermal characterization parameter. This estimated junction temperature can then be compared with a junction temperature specification. A component power estimate is required.

Ψ_{JT} is the junction-to-top thermal characterization parameter where T_{Top} is the temperature at the top center of the package as described in [3] and [7].

$$\Psi_{JT} = \frac{T_J - T_{Top}}{P}$$

P is the total power (heat) dissipated in the chip. The power may leave the chip through any thermal path, not just the top of the package.

Ψ_{JB} is the junction-to-board thermal characterization parameter where T_{Board} is the temperature measured on or near the component lead as described above for θ_{JB} and in [6] and [9].

$$\Psi_{JB} = \frac{T_J - T_{Board}}{P}$$

P is the total power (heat) dissipated in the chip. The power may leave the chip through any thermal path, not just the board.

Thermal characterization parameters are not thermal resistances. This is because when the parameter is measured, the component power is flowing out of the component through multiple paths. Ψ_{JB} is lower than or approximately equal to θ_{JB}. Ψ_{JT} is often significantly lower than θ_{JCtop}. For example, Ψ_{JT} might be 1 °C/W when θ_{JCtop} is 6 °C/W.

Prior to having hardware on which to measure temperatures for a component application, Ψ_{JB} may help provide a good application junction temperature estimate if an appropriate board temperature can be estimated and if a heat sink is not used.

5.2 JESD51 standardized thermal values (cont'd)

5.2.3 Ψ_{JT} and Ψ_{JB} thermal characterization parameters (cont'd)

Once application hardware is available, Ψ_{JT} or Ψ_{JB} values may be used with package top or board temperature measurements respectively to provide good junction temperature estimates. When the component power is not precisely known, the use of Ψ_{JT} may provide a more accurate T_J estimate. This is because the top surface temperature of the component is generally closer to the junction temperature than is the board temperature. Therefore, Ψ_{JT} is smaller than Ψ_{JB} and there is less absolute temperature prediction error. This is true even though the Ψ_{JT} standard deviation may be a significant percentage of the average Ψ_{JT} value.

Using Ψ_{JT} or Ψ_{JB} values together with package top or board temperature measurements in a system requires good temperature measurement technique, comparable to that used when the supplier measured Ψ_{JT} or Ψ_{JB}. For the top temperature, a 36 gauge Type J or K thermocouple or a 40 gauge Type T thermocouple is recommended, attached to the center of the top surface of the package with a thermally conductive epoxy. The center location is particularly important for plastic packages. The board temperature is measured using a 40 gauge thermocouple soldered to a lead foot where the lead is attached to the board, at the edge of the package footprint, at the center of one side of the package. For an area array package, the thermocouple is soldered to a board trace within 1 mm of the package body. A Type T thermocouple is recommended because it is easily soldered. Cover the thermocouple junction and about 1 mm of wire with a thermally conductive adhesive. More details are given in [3] and [7] for the top temperature and in [7] and [9] for the package board temperature.

When a heat sink or added heat spreader is present, neither Ψ_{JT} nor Ψ_{JB} can be used to estimate the junction temperature. It can be approximated using θ_{JCtop}, measuring the heat sink temperature in the application as close to the package interface as possible, and accounting for the temperature difference across the heat sink to case interface. Alternatively, some suppliers may provide a junction-to-sink Ψ_{JS} thermal parameter that may be used analogously to Ψ_{JT}, recognizing that the Ψ_{JS} value is dependent on the package-to-heat sink interface.

5.2.4 Compact models and detailed models

Standardized thermal resistances and thermal characterization parameters don't accurately predict the thermal performance of a component in a user's application. If more accuracy is desired, users may wish to investigate analyzing a component in their application using compact models or detailed models.

A two-resistor compact model is the simplest model. θ_{JCtop} and θ_{JB} are placed in a resistor network as shown in Figure 2 and described in JESDxx-yy [13]. The junction node is connected to the top case node by θ_{JCtop} and to the board node by θ_{JB}. For packages which are designed to inject heat directly into the ground plane of the board such as exposed tab packages, the user may consider replacing θ_{JB} by $\theta_{JCbottom}$. The two-resistor compact model can be used in hand calculations or several simulation models including resistor network solvers, conduction-based board level thermal simulation tools, and computational fluid dynamics (CFD) codes. While the simplicity and intuitiveness of a two-resistor model are attractive, accuracy remains a concern. Users should exercise care in using two-resistor model data for predicting package temperatures.

5.2 JESD51 standardized thermal values (cont'd)

5.2.4 Compact models and detailed models (cont'd)

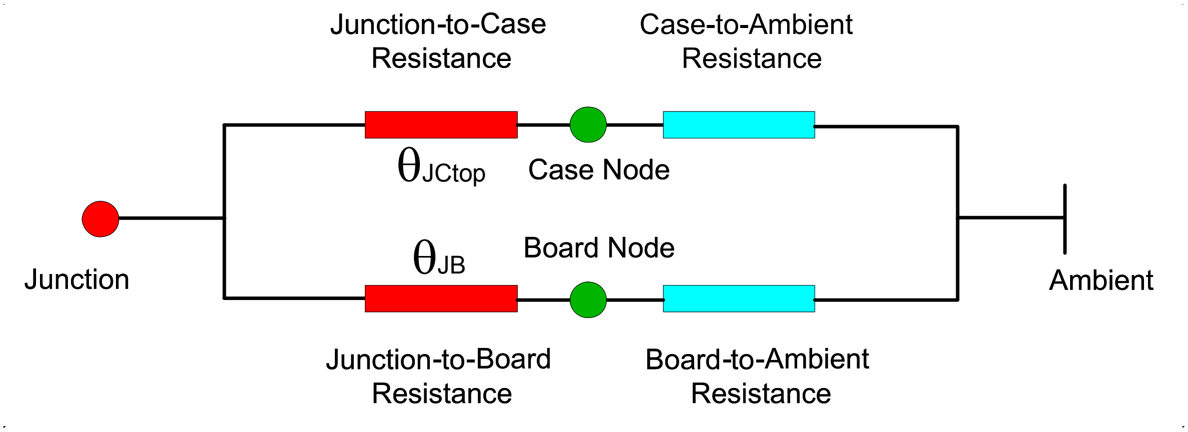

Figure 2 — Equivalent thermal resistance diagram of the two-resistor model on a PCB

DELPHI compact models are described in JESDxx-zz [14] and an example is shown in Figure 3. The models are not based on the measured thermal resistances or thermal characterization parameters described previously, though these may be used to check the model. The connections between nodes in a DELPHI compact model are mathematical constructs, not thermal resistances; they do not correspond to a physical thermal resistance between the two nodes. The DELPHI compact models are based on analysis and are intended to be provided by component suppliers. Some users may wish to generate their own DELPHI compact models using either their own tools or commercial codes. DELPHI compact models can be used with resistor network solvers, conduction-based board level thermal simulation tools, and CFD codes.

Detailed models involve representing all the heat conduction paths in the model. This is generally done using conduction codes or CFD codes. Detailed models are required to generate DELPHI compact models.

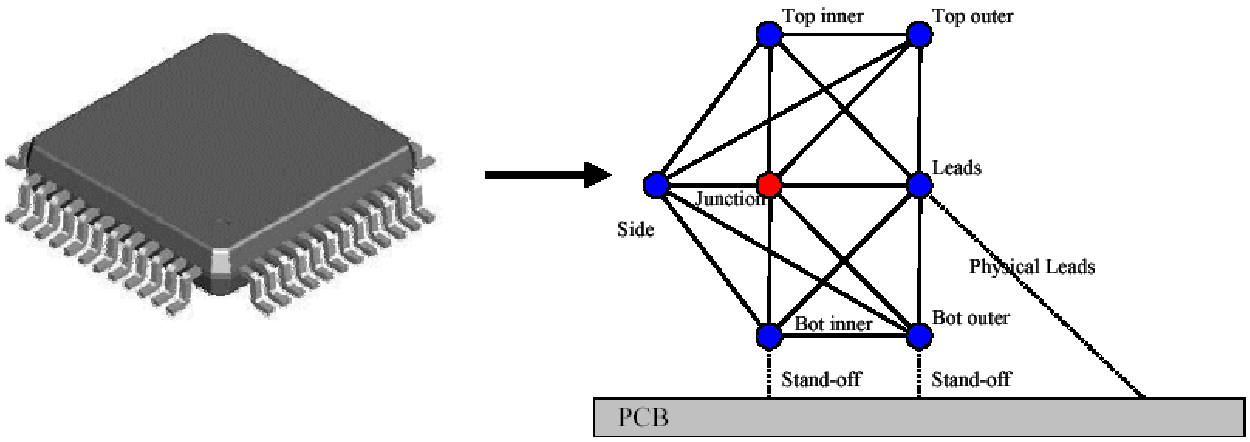

Figure 3 — Possible DELPHI node topology for a PQFP package

5.3 Selected variables affecting thermal performance

Variables like package construction, printed circuit board design and size, and die size affect the thermal results. Examples are given to illustrate this point. Thermal performance values are included to make the illustrations more meaningful, but the values should not be used for any other purpose. The package type is also given to make the illustrations more meaningful, but the effect of the variable is not limited to the package type used.

5.3.1 Package construction

Package thermal performance can change significantly with seemingly small changes in package construction. Results for one package cannot be applied to a second similar package without investigating the effect of the differences on thermal performance.

Figure 4 demonstrates this for two plastic ball grid array (PBGA) packages. Both are 35 mm, 388 lead PBGA packages, built and tested by one company on single layer (1s) printed circuit boards, but the package laminate substrates are different. The first substrate has only two signal planes while the second substrate has two signal and two power planes. The added copper significantly improves the thermal performance of the package with the 2s2p laminate substrate.

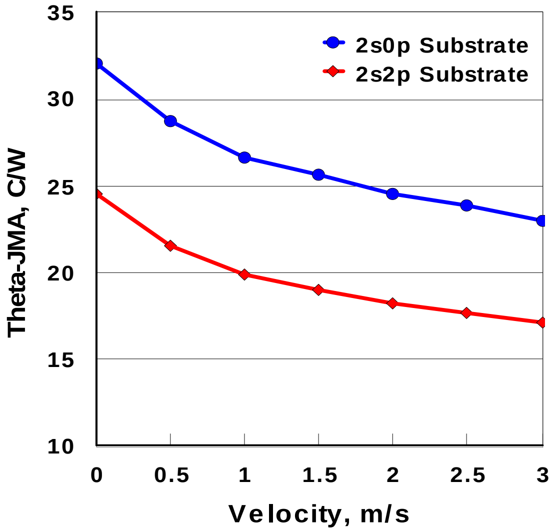

Figure 4 — Effect of Package Construction on Thermal Results

5.3.2 Printed circuit board design

The thermal performance of an electronic package may vary significantly depending on whether it is tested on the JESD51 1s or 2s2p board (see Table 1, note 3 for an explanation of the two boards; JEDEC does not make thermal test boards available). Components will run hotter on the 1s board because it has less copper to conduct and spread the heat and they will run cooler on the 2s2p board because it has more copper. This is best understood if package thermal data is available for both boards.

The design of the JESD51 defined test boards is required to limit the PCB-related variation in measured θ_{JA} for a given package geometry when the test board is within the minimum to maximum range of all board design parameters. Achieving this requires controlling the heat-sinking characteristics of the board by controlling the board design parameters such as the area of the test board, the amount of copper traces on the test board, and the resulting trace fan-out area. For example, JESD51 test board signal layer traces are generally 0.070 mm (2 oz/ft^2) finished copper thickness though application boards generally have thinner traces. With thinner traces, the standard thermal results would have been too sensitive to normal plating thickness variations.

5.3 Selected variables affecting thermal performance (cont'd)

5.3.2 Printed circuit board design (cont'd)

To avoid confusion, it is important that the test board be defined with all package thermal results. Some of the JESD51 environment standards indicate which JESD51 board is to be used. The θ_{JB} junction-to-board standard (JESD51-8, section 4.1 [9]) requires that the test be run using a 2s2p board to increase the heat transfer to the board and to provide a more uniform board temperature. The natural convection (still air) standard (JESD51-2, sections 1.2 & 2.5 [3]) and the forced convection (moving air) standard (JESD51-6, section 4.2 [7]) presume that the tests are run using a 1s board unless the reported test conditions indicate otherwise.

Package suppliers may choose which boards to use. For example, a 1s board may not be practical for high lead count components. Also, 1s boards will not properly reflect the thermal benefits of packages which are designed to inject heat directly into the ground plane of the board. Such packages include BGA packages with thermal balls and exposed pad lead-frame packages.

Figure 5 demonstrates the effect of the test board on thermal results for a 35 mm, 388 lead plastic ball grid array (PBGA) package with a 2s0p laminate substrate.

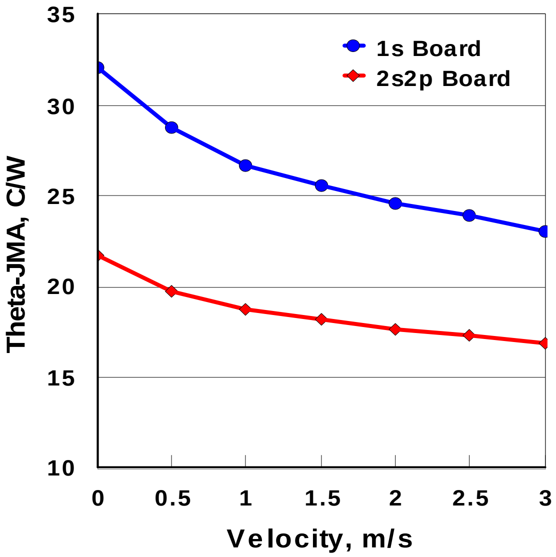

Figure 5 — Effect of Board Construction on Thermal Results

The thermal performance of an electronic package on the 1s and 2s2p boards brackets the performance of a package in many applications. Nonetheless, the θ_{JA} and θ_{JMA} tests are not intended to simulate application conditions. Figure 6 shows that package results on a 1s board may be closer than those on a 2s2p board to the results for an application board with many tightly grouped components. However, the Figure 6a data for neither single-component board accurately represents the results for the highest temperature package on the Figure 6b multiple-component boards.

Figure 6a shows single-component test data on the 2s2p and 1s test boards. Figure 6b shows data for two simulated applications: a board with eight packages on one board side, and a board with eight packages on both sides (16 packages). For each board, the θ_{JMA} result for the highest temperature package is shown. The device is a 14 mm x 22 mm PBGA memory package. Multiple packages are arranged in a closely spaced (4 row) x (2 column) array. The package power is 1 W each and the θ_{JMA} wind tunnel velocity is 0 m/s.

5.3 Selected variables affecting thermal performance (cont'd)

5.3.2 Printed circuit board design (cont'd)

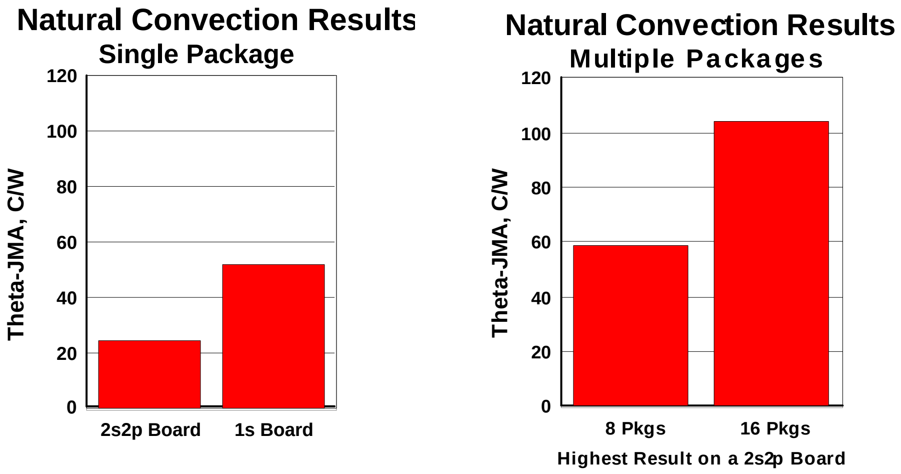

Figure 6a Figure 6b

Figure 6 — Comparison of Single Package and Multiple Package Thermal Resistances

5.3.3 Printed circuit board size

The printed circuit board around a package provides surface area to convect package heat to the air and radiate heat to nearby surfaces. The copper contribution of the JESD51 2s2p test board aids this heat transfer by spreading heat away from the package. The package thermal performance will be better on a 2s2p JESD51-size test board than on a smaller 2s2p test board. Package results on smaller boards may be closer to system level performance when the package in the system has other heat sources around it. Board size is generally best addressed with modeling because testing using a large number of test board sizes would be expensive and time consuming.

Figure 7 illustrates the effect of board size on package thermal performance. A test board with nearly eight times the surface area of the test package was cut down in steps until the board area was less than two times the package area. θ_{JMA} increased as the test board got smaller, particularly at low air velocity. These results are for a 40 mm tape ball grid array (TBGA) package on a 4s2p board.

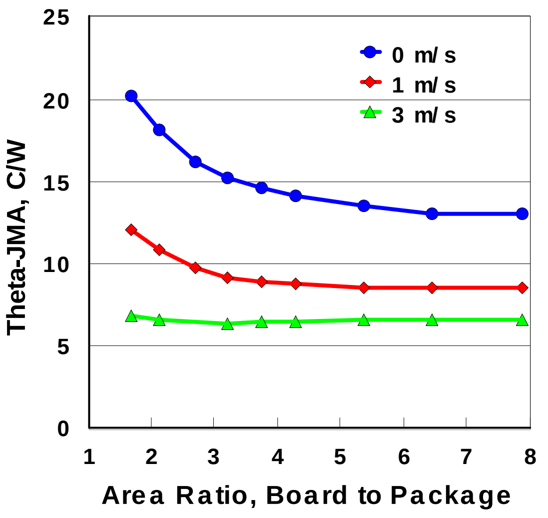

Figure 7 — Effect of PCB Size on Thermal Results

5.3 Selected variables affecting thermal performance (cont'd)

5.3.4 Die size

Die or chip size often has a significant effect on package thermal performance so it must be reported with the thermal data (see [5] and Table 5). A larger die reduces thermal resistances because the chip power is already spread over a larger area and therefore the larger die has a lower die heat flux (commonly expressed in watts per square centimeter). However, reduced die sizes are popular because the cost is lower.

The effect of die size on thermal performance of two packages is demonstrated in Figure 8. Figure 8a shows results for a 13 mm PBGA package tested on both 1s and 2s2p boards. Figure 8b is for a 36 mm flip chip ceramic quad flatpack (CQFP) package on a 1s non-JESD51 test board; both bare die and flat plate aluminum heat spreader results are shown. Both figures show data at an air velocity of 1 m/s. The die size effect is more pronounced for the plastic part. The ceramic part with the metal heat spreader is less affected by chip size.

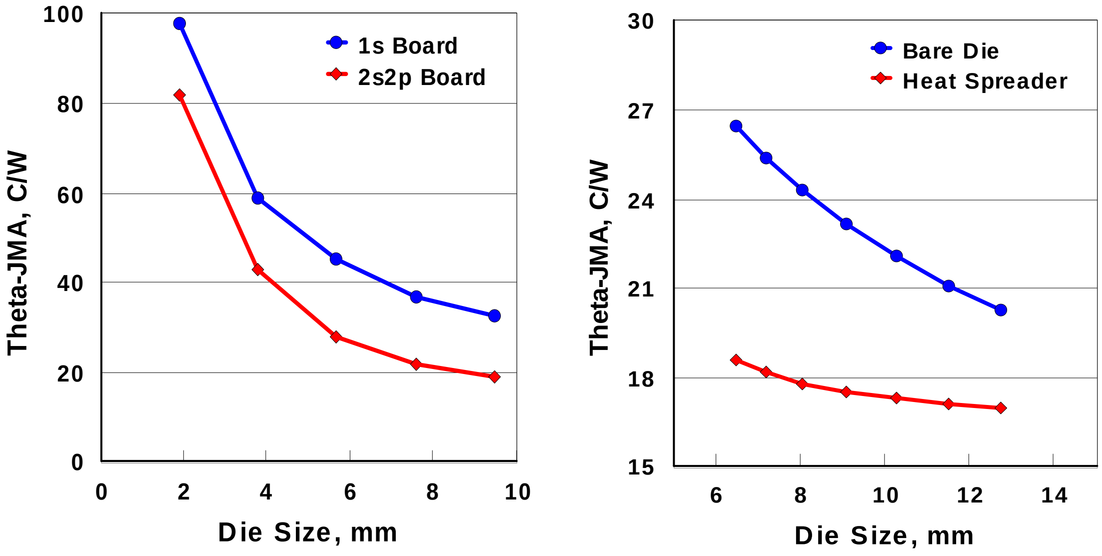

Figure 8a

Figure 8b

Figure 8 — Effect of Die Size on Thermal Results

To accurately compare package thermal results, the die size should be the same. Customers may want to request that thermal results be extrapolated to the die size of interest.

5.3.5 Die power level

Package thermal results may show variations with die power level because heat transfer characteristics change with temperature. For example, both natural convection and thermal radiation increase with increasing temperature difference between the package surface and the surroundings. Conversely, the thermal conductivity of a silicon chip decreases with increasing temperature. The net result of these effects is a reduction or improvement in package thermal performance numbers at higher die power levels that is most noticeable at low air velocity below 0.5 m/s. Partly because of these effects, JESD51 environment standards [3] and [7] indicate what power is to be used during testing.

5.3 Selected variables affecting thermal performance (cont'd)

5.3.6 Multi-Chip Packages (MCP)

The thermal performance of packages with more than one chip is more complicated. Standard thermal resistance θ values and thermal parameter Ψ values cannot be used. A number of approaches have been suggested in the literature, sometimes in connection with a specific multi-chip package type. JEDEC is evaluating them. Detailed modeling is often used.

6 Information to be reported

Each of the JESD51 standards has a table at the end that tells the component supplier what test information is to be reported. Key elements of those tables are provided here. Refer to the individual standards for the complete tables. Refer to section 4 of this document for additional information about reporting results. Units of thermal resistance in °C/W are numerically equivalent to thermal resistance values in K/W.

6.1 Environments

Table 2 — JESD51-2 Natural Convection Test Conditions and Data Parameters [3]

Measurement Area	Condition Parameters	Data Parameters and Results
Device Identification *		Device Identification Date
Environmental	Test Board Orientation Enclosure (box) Size	
Measurements *		Power P_H (watts) θ_{JA} (°C/W)
Package Case Measurement (Optional)	Thermocouple wire gauge # (AWG) Thermocouple type (T, J, or K) Attachment Method	Ψ_{JT} (°C/W)

* These items and the order of the items have been modified from [3] to reflect later JESD51 standards. Ψ_{JB} was not included in the natural convection standard; it had not yet been defined. It may be added in the future. Ψ_{JB} can be measured in the natural convection environment, but it is normally measured on a 2s2p board, and in the forced convection environment, including the zero forced convection condition [7].

Table 3 — JESD51-6 Forced Convection Test Conditions and Data Parameters [7]

Measurement Area	Condition Parameters	Data Parameters and Results
Device Identification		Device Identification Date
Environmental	Test Board Specification Wind Tunnel Type Wind Tunnel Test Section Dimensions Flow Orientation Test Board Orientation	
For Each Mean Flow Velocity		(m/s or ft/min)
Measurements *		Power P_H (watts) θ_{JMA} (°C/W)
Package Case Measurement (Optional) *	Thermocouple wire gauge # (AWG) Thermocouple type (T, J, or K) Attachment Method	Ψ_{JT} (°C/W)
Board Measurement (Optional)		Ψ_{JB} (°C/W)

* These items have been modified from [7] to reflect other JESD51 standards.

6 Information to be reported (cont'd)

6.1 Environments (cont'd)

Table 4 — JESD51-8 Junction-to-Board Test Conditions and Data Parameters [9]

Measurement Area	Condition Parameters	Data Parameters and Results
Device Identification		Device Identification Date
Environmental	Cold Plate Drawing number Test Board Specification (& dwg #) Thermocouple type and gauge Thermocouple attachment location	
Measurements		Power P_H (watts) θ_{JB} (°C/W)

6.2 Chips

Table 5 — JESD51-4 Wire Bond Chip Test Conditions and Data Parameters [5]

Measurement Area	Condition Parameters	Data Parameters
Device Construction	Chip name & number Chip material Chip size Chip thickness Heating source area coverage %	
For Single Unit Chip	Temperature Sensor Location	
For Multiple Unit Chip	Base chip unit size Array topography Powered up units Temperature sensor locations	

6.3 Boards

JESD51-3 [4] and JESD51-7 [8] apply to leaded surface mount (SMT) packages like plastic quad flat-packs (PQFPs), and define the 1s and 2s2p test boards respectively.

Table 6 — JESD51-3 Low Thermal Conductivity Leaded SMT Test Board Parameters [4]

Dimension	Specification	User
Board Thickness	1.60 mm ± 10% *	
Board Dimension (pkg length < 27 mm)	76.2 mm x 114.3 mm	
Board Dimension (27 mm ≤ pkg length ≤ 48 mm)	101.6 mm x 114.3 mm	
Board material	FR-4	
Trace Copper Thickness	0.071 mm ± 20%	
Trace Width, Finished	0.25 mm ± 10% for ≥ 0.50 mm pin pitch Lead width for < 0.50 mm pin pitch	
Trace Coverage Area (Total)		
* This item has been modified from [4] to reflect later JESD51 standards.		

6 Information to be reported (cont'd)

6.3 Boards (cont'd)

Table 7 — JESD51-7 High Thermal Conductivity Leaded SMT Test Board Parameters [8]

Dimension	Specification	User
Board Finish Thickness	1.60 mm ± 10%	
Board Dimension (pkg length < 27 mm)	76.2 mm x 114.3 mm	
Board Dimension (27 mm ≤ pkg length ≤ 48 mm)	101.6 mm x 114.3 mm	
Board material	FR-4	
Trace Copper Thickness	0.070 mm ± 20%	
Trace Width, Finished	0.25 mm ± 10% for ≥ 0.50 mm pin pitch Lead width for < 0.50 mm pin pitch	
Trace Coverage Area (Total)		
Power/Ground Thickness	35 µm (1oz) copper +0/-20%	

JESD51-5 [6] extends the test boards to packages with direct thermal attach mechanisms like deep down-set exposed pad packages and thermally tabbed packages. Generally this applies to the SMT boards defined in [4] and [8] covered in Tables 6 and 7.

Table 8 — JESD51-5 Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms [6]

Dimension	Specification	User
Attachment Pad Size (single PCB)	Attach geometry size or less than 1 mm larger	
Attachment Array Size (nested PCB)	Size of largest attach geometry	
Array Trace Square Size	1.0 mm x 1.0 mm	
Array Trace Spacing	0.2 mm	
No. of Vias to Top Buried Layer		

JESD51-9 [10] defines test boards for area array SMT packages like ball grid array (BGA) packages. Both 1s and 2s2p test boards are included, as are requirements for dealing with thermal balls and vias.

TABLE 9 — JESD51-9 Area Array SMT Test Board Parameters [10]

Dimension	Specification	User
Board Finish Thickness	1.60 mm ± 10%	
Board Dimension (± 0.25 mm)	101.5 mm x 114.5 mm [PKG ≤ 40 mm] 127.0 mm x 139.5 mm [40 < PKG ≤ 65 mm] 152.5 mm x 165.0 mm [65 < PKG ≤ 90 mm]	
Board material	FR-4	
Trace Copper Thickness	70 µm ± 20% for > 0.5 mm ball pitch 50 µm ± 20% for ≤ 0.5 mm ball pitch	
Trace Width, Finished	36% to 44% of ball pitch for pitches > 0.5 mm 45% to 55% of ball pitch for pitches ≤ 0.5 mm	
Trace Coverage Area (Total)		
Multilayer (buried power/ground)	Yes/no	
Power/Ground Thickness	35 µm (1oz) copper +0/-20%	
No. of Thermal Ball Pads		
No. of Thermal Vias		
No. of Thermal Vias to Top Plane	(2s2p PCB only)	
No. of Thermal Vias to Bottom Plane	(2s2p PCB only)	

6 Information to be reported (cont'd)

6.3 Boards (cont'd)

JESD51-10 [11] and JESD51-11 [12] define test boards for through-hole leaded packages like pin grid array packages (PGAs). [11] covers perimeter leaded packages and [12] covers area array leaded packages. Both 1s and 2s2p test boards are included in both standards.

Table 10 — JESD51-10 Through-Hole Perimeter Leaded Package Test Board Parameters [11]

Dimension	Specification	User
Board Finish Thickness	1.60 mm ± 10%	
Board Dimension (± 0.25 mm)	101.5 mm x 114.5 mm [PKG ≤ 40 mm] 127.0 mm x 139.5 mm [40 < PKG ≤ 65 mm] 152.5 mm x 165.0 mm [65 < PKG ≤ 90 mm]	
Board material	FR-4	
Trace Copper Thickness	70 μm ± 20%	
Trace Width, Finished	0.25 mm ± 10%	
Trace Coverage Area (Total)		
Multilayer (buried power/ground)	Yes/no	
Power/Ground Thickness	35 μm (1oz) copper +0/-20%	
Number of Thermal Pins		

Table 11 — JESD51-11 Through-Hole Area Array Leaded Package Test Board Parameters [12]

Dimension	Specification	User
Board Finish Thickness	1.60 mm ± 10%	
Board Dimension (± 0.25 mm)	101.5 mm x 114.5 mm [PKG ≤ 40 mm] 127.0 mm x 139.5 mm [40 < PKG ≤ 65 mm] 152.5 mm x 165.0 mm [65 < PKG ≤ 90 mm]	
Board material	FR-4	
Trace Copper Thickness	70 μm ± 20%	
Trace Width, Finished	From 36% to 44% of pin pitch	
Trace Coverage Area (Total)		
Multilayer (buried power/ground)	Yes/no	
Power/Ground Thickness	35 μm (1oz) copper +0/-20%	

6.4 Measurement Methods

All key electrical measurement elements listed in JESD51-1 [2] are included in each of the environment standards [3, 7, 9, 13].

Standard Improvement Form **JEDEC JESD51-12**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

☐ Requirement, clause number ________________

☐ Test method number ________ Clause number ________________

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other ________________________________

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2. Recommendations for correction:

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3. Other suggestions for document improvement:

Submitted by

Name: ____________________ Phone: ______________

Company: ____________________ E-mail: ______________

Address: ____________________

City/State/Zip: ____________________ Date: ______________

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